body or other region through which current passes during operation. As described above, the region may be a lightly doped p-type ring (e.g., p-type epitaxial ring). The semiconductor device may have an SOI substrate, an open drain structure or other diminished drift region, and/or other features to improve the breakdown voltage level of a transistor device, such as a p-channel LDMOS transistor device. The breakdown protection region may allow such improvements to be achieved by preventing breakdown along the device area periphery. For example, the ring may reduce the E-field stress at a DTI corner, while also effectively lowering the pinning potential to reduce the E-field stress at drain. BVdss breakdown voltage levels of about 125 Volts or more may be achieved through, for instance, optimization of the width of the breakdown protection ring or region.

In a first aspect, a device includes a semiconductor substrate, source and drain regions disposed in the semiconductor substrate and having a first conductivity type, a body region disposed in the semiconductor substrate, having a second conductivity type, and in which the source region is disposed, a drift region disposed in the semiconductor substrate, having the first conductivity type, and through which charge carriers drift during operation upon application of a bias voltage between the source and drain regions, a device isolation region disposed in the semiconductor substrate and laterally surrounding the body region and the drift region, and a breakdown protection region disposed between the device isolation region and the body region and having the first conductivity type.

In a second aspect, an electronic apparatus includes a semiconductor substrate and a transistor disposed in the semiconductor substrate. The transistor includes first and second semiconductor regions having a first conductivity type, a third semiconductor region having a second conductivity type and through which current flows between the first and second semiconductor regions during operation, a device isolation region laterally surrounding the first, second, and third semiconductor regions, a breakdown protection region disposed between the device isolation region and the third semiconductor region and having the first conductivity type, and a buried layer extending laterally across the first semiconductor region, the second semiconductor region, and the third semiconductor region and having the second conductivity type.

In a third aspect, a method of fabricating a transistor in a semiconductor substrate includes forming a device isolation region in the semiconductor substrate, implanting dopant in a first region of the semiconductor substrate to form a drift region, forming source and drain regions in second and third regions of the semiconductor substrate, respectively, and implanting dopant to form a body region in which the source region is disposed and to form a breakdown protection region disposed between the device isolation region and the body region.

Semiconductor devices with a conductive gate electrode positioned over a dielectric or other insulator may be considered MOS devices, despite the lack of a metal gate electrode and an oxide gate insulator. Accordingly, the terms metal-oxide-semiconductor and the abbreviation "MOS" may be used even though such devices may not employ metals or oxides but various combinations of conductive materials, e.g., metals, alloys, silicides, doped semiconductors, etc., instead of simple metals, and insulating materials other than oxides (e.g., nitrides, oxy-nitride mixtures, etc.). Thus, as used herein, the terms MOS and LDMOS are intended to include such variations.

The present invention is defined by the following claims and their equivalents, and nothing in this section should be taken as a limitation on those claims. Further aspects and advantages of the invention are discussed above in conjunction with the preferred embodiments and may be later claimed independently or in combination.

While the invention has been described above by reference to various embodiments, it should be understood that many changes and modifications may be made without departing from the scope of the invention. It is therefore intended that the foregoing detailed description be regarded as illustrative rather than limiting, and that it be understood that it is the following claims, including all equivalents, that are intended to define the spirit and scope of this invention.

The invention claimed is:

1. A device comprising:

a semiconductor substrate;

source and drain regions disposed in the semiconductor substrate and having a first conductivity type;

a body region disposed in the semiconductor substrate, having a second conductivity type, and in which the source region is disposed;

a drift region disposed in the semiconductor substrate, having the first conductivity type, and through which charge carriers drift during operation upon application of a bias voltage between the source and drain regions;

a device isolation region disposed in the semiconductor substrate and laterally surrounding the body region and the drift region; and

a breakdown protection region disposed between the device isolation region and the body region and having the first conductivity type;

wherein the breakdown protection region comprises an electrically floating well disposed between the device isolation region and the body region;

wherein the breakdown protection region has a width at a surface of the semiconductor substrate in a lateral direction that establishes a spacing between the body region and the device isolation region, the width falling in a range from 1.0 microns to 2.0 microns so that the breakdown protection region improves a breakdown voltage level of the device by preventing charge inversion from occurring in the body region along the device isolation region; and

wherein the first conductivity type is p-type and the second conductivity type is n-type.

2. The device of claim **1**, wherein the breakdown protection region is ring-shaped and laterally surrounds the body region.

3. The device of claim **1**, wherein the breakdown protection region is disposed along, and contiguous with, an inner boundary of the device isolation region.

4. The device of claim **1**, wherein:

the semiconductor substrate comprises an epitaxial layer in which the body region and the drift region are disposed; and

the breakdown protection region is a portion of the epitaxial layer outside of dopant profiles of the body region and the drift region.

5. The device of claim **1**, further comprising a buried layer disposed in the semiconductor substrate, extending laterally across the body region, the drift region, and the breakdown protection region, and having the second conductivity type.

6. The device of claim **5**, further comprising a buried oxide layer disposed in the semiconductor substrate, over which the buried layer is disposed, and disposed at a depth to which the device isolation region reaches.